SYNCHRONOUS DRAM MODULE

MT36LSDF6472G - 512MB
MT36LSDF12872G - 1GB

For the latest data sheet, please refer to the Micron Web site: www.micron.com/datasheets

FEATURES

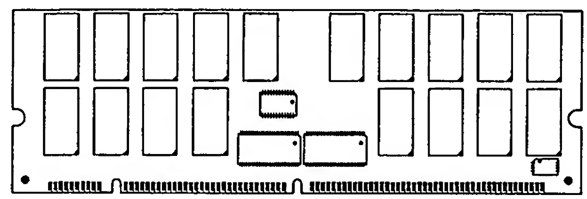
- JEDEC-standard, 168-pin, dual in-line memory module (DIMM)
- PC100 and PC133 compliant
- FBGA-packaged SDRAM components
- Registered inputs with one-clock delay
- Phase-lock loop (PLL) clock driver to reduce loading
- Utilizes 100 MHz and 133 MHz SDRAM components
- ECC-optimized pinout
- Single +3.3V ±0.3V power supply
- Fully synchronous; all signals registered on positive edge of PLL clock
- Internal pipelined operation; column address can be changed every clock cycle
- Internal SDRAM banks for hiding row access/precharge
- Programmable burst lengths: 1, 2, 4, 8, or full page
- Auto Precharge and Auto Refresh Modes
- Self Refresh Mode
  512 MB: 64ms, 4,096-cycle refresh; 1GB: 64ms, 8,192 cycle refresh
- LVTTL-compatible inputs and outputs
- Serial presence-detect (SPD)
- Minimum case airflow of 1 meter/second recommended

OPTIONS — MARKING

OPTIONS	MARKING
• Package	
168-pin DIMM (gold)	G
• Frequency/CAS Latency*	
133 MHz/CL = 2	-13E
133 MHz/CL = 3	-133
100 MHz/CL = 2	-10E

*An extra clock cycle will be incurred when the module is in registered mode.

168-Pin DIMM



ADDRESS TABLE

	512MB Module	1GB Module
Refresh Count	4K	8K
Device Banks	4 (BA0, BA1)	4 (BA0, BA1)
Device Configuration	32 Meg x 4	64 Meg x 4
Row Addressing	4K (A0–A11)	8K (A0–A12)
Column Addressing	2K (A0–A9,A11)	2K (A0–A9,A11)
Module Banks	2 (S0,S2; S1,S3)	2 (S0,S2; S1,S3)

DEVICE TIMING

Module Markings	PC100 CL - tRCD - tRP	PC133 CL - tRCD - tRP
-13E	2 - 2 - 2	2 - 2 - 2
-133	2 - 2 - 2	3 - 3 - 3
-10E	2 - 2 - 2	NA

PART NUMBERS

PART NUMBER	CONFIGURATION	SYSTEM BUS SPEED
MT36LSDF6472G-13E__	64 Meg x 72	133 MHz
MT36LSDF6472G-133__	64 Meg x 72	133 MHz
MT36LSDF6472G-10E__	64 Meg x 72	100 MHz
MT36LSDF12872G-13E__	128 Meg x 72	133 MHz
MT36LSDF12872G-133__	128 Meg x 72	133 MHz
MT36LSDF12872G-10E__	128 Meg x 72	100 MHz

NOTE: The designators for component and PCB revision are the last two characters of each part number. Consult factory for current revision codes. Example: MT36LSDF6472G-133B1

PIN ASSIGNMENT (168-PIN DIMM FRONT)

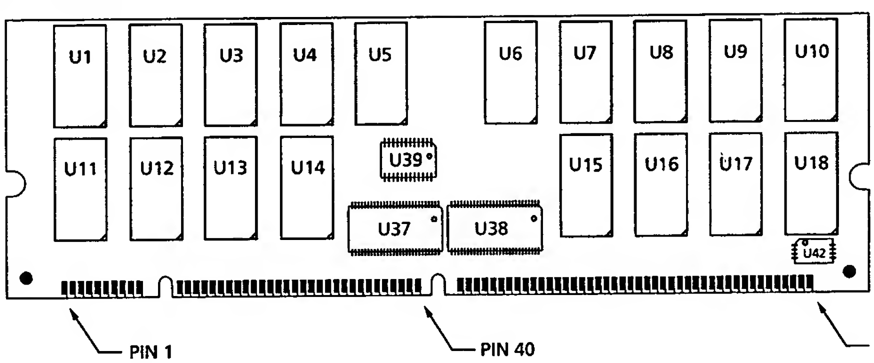
PIN	SYMBOL	PIN	SYMBOL	PIN	SYMBOL	PIN	SYMBOL
1	Vss	22	CB1	43	Vss	64	Vss
2	DQ0	23	Vss	44	NC	65	DQ21
3	DQ1	24	NC	45	S2#	66	DQ22
4	DQ2	25	NC	46	DQMB2	67	DQ23
5	DQ3	26	VDD	47	DQMB3	68	Vss
6	VDD	27	WE#	48	NC	69	DQ24
7	DQ4	28	DQMB0	49	VDD	70	DQ25
8	DQ5	29	DQMB1	50	NC	71	DQ26
9	DQ6	30	S0#	51	NC	72	DQ27
10	DQ7	31	NC	52	CB2	73	VDD
11	DQ8	32	Vss	53	CB3	74	DQ28
12	Vss	33	A0	54	Vss	75	DQ29
13	DQ9	34	A2	55	DQ16	76	DQ30
14	DQ10	35	A4	56	DQ17	77	DQ31
15	DQ11	36	A6	57	DQ18	78	Vss
16	DQ12	37	A8	58	DQ19	79	CK2
17	DQ13	38	A10	59	VDD	80	NC
18	VDD	39	BA1	60	DQ20	81	WP
19	DQ14	40	VDD	61	NC	82	SDA
20	DQ15	41	VDD	62	NC	83	SCL
21	CB0	42	CK0	63	NC	84	VDD

PIN ASSIGNMENT (168-Pin DIMM BACK)

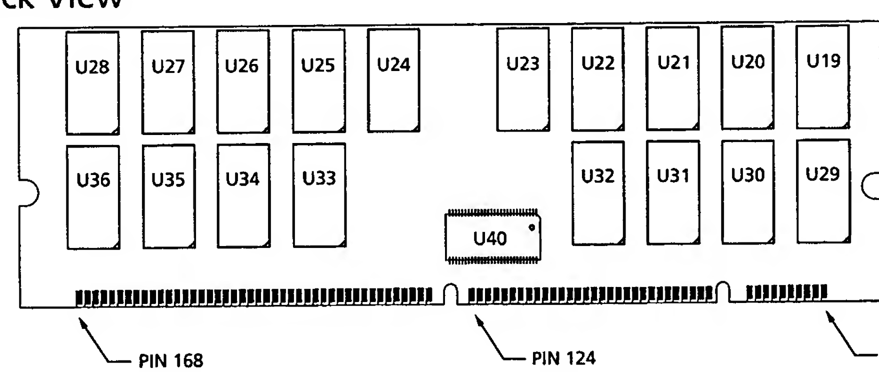
PIN	SYMBOL	PIN	SYMBOL	PIN	SYMBOL	PIN	SYMBOL
85	Vss	106	CB5	127	Vss	148	Vss
86	DQ32	107	Vss	128	CKE0	149	DQ53
87	DQ33	108	NC	129	S3#	150	DQ54
88	DQ34	109	NC	130	DQMB6	151	DQ55
89	DQ35	110	VDD	131	DQMB7	152	Vss
90	VDD	111	CAS#	132	NC	153	DQ56
91	DQ36	112	DQMB4	133	VDD	154	DQ57
92	DQ37	113	DQMB5	134	NC	155	DQ58
93	DQ38	114	S1#	135	NC	156	DQ59
94	DQ39	115	RAS#	136	CB6	157	VDD
95	DQ40	116	Vss	137	CB7	158	DQ60
96	Vss	117	A1	138	Vss	159	DQ61
97	DQ41	118	A3	139	DQ48	160	DQ62
98	DQ42	119	A5	140	DQ49	161	DQ63
99	DQ43	120	A7	141	DQ50	162	Vss
100	DQ44	121	A9	142	DQ51	163	CK3
101	DQ45	122	BA0	143	VDD	164	NC
102	VDD	123	A11	144	DQ52	165	SA0
103	DQ46	124	VDD	145	NC	166	SA1
104	DQ47	125	CK1	146	NC	167	SA2
105	CB4	126	NC/A12	147	REGE	168	VDD

*Pin 126 is NC for 512MB module, or A12 for 1GB module

Front View



Back View



GENERAL DESCRIPTION

The MT36LSDF6472G and MT36LSDF12872G are high-speed CMOS, dynamic random-access, 512MB and 1GB memory modules organized in x72 (ECC) configurations. These modules use internally configured quad-bank SDRAMs with a synchronous interface (all signals are registered on the positive edge of clock signal CK0).

Read and write accesses to the SDRAM modules are burst oriented; accesses start at a selected location and continue for a programmed number of locations in a programmed sequence. Accesses begin with the registration of an ACTIVE command, which is then followed by a READ or WRITE command. The address bits registered coincident with the ACTIVE command are used to select the device bank and row to be accessed (BA0, BA1 select the device bank; A0-A11 for 512MB/A0-A12 for 1GB, select the device row). The address bits registered coincident with the READ or WRITE command are used to select the starting column location for the burst access.

These modules provide for programmable READ or WRITE burst lengths of 1, 2, 4, or 8 locations, or full page, with a burst terminate option. An auto precharge function may be enabled to provide a self-timed row precharge that is initiated at the end of the burst sequence.

These modules use an internal pipelined architecture to achieve high-speed operation. This architecture is compatible with the $2n$ rule of prefetch architectures, but it also allows the column address to be changed on every clock cycle to achieve a high-speed, fully random access. Precharging one device bank while accessing one of the other three device banks will hide the PRECHARGE cycles and provide seamless, high-speed, random-access operation.

These modules are designed to operate in 3.3V, low-power memory systems. An auto refresh mode is provided, along with a power-saving, power-down mode. All inputs and outputs are LVTTL-compatible.

SDRAM modules offer substantial advances in DRAM operating performance, including the ability to synchronously burst data at a high data rate with automatic column-address generation, the ability to interleave between device banks in order to hide precharge time, and the capability to randomly change column addresses on each clock cycle during a burst access. For more information regarding SDRAM operation, refer to the 128Mb and 256Mb SDRAM data sheets.

PLL AND REGISTER OPERATION

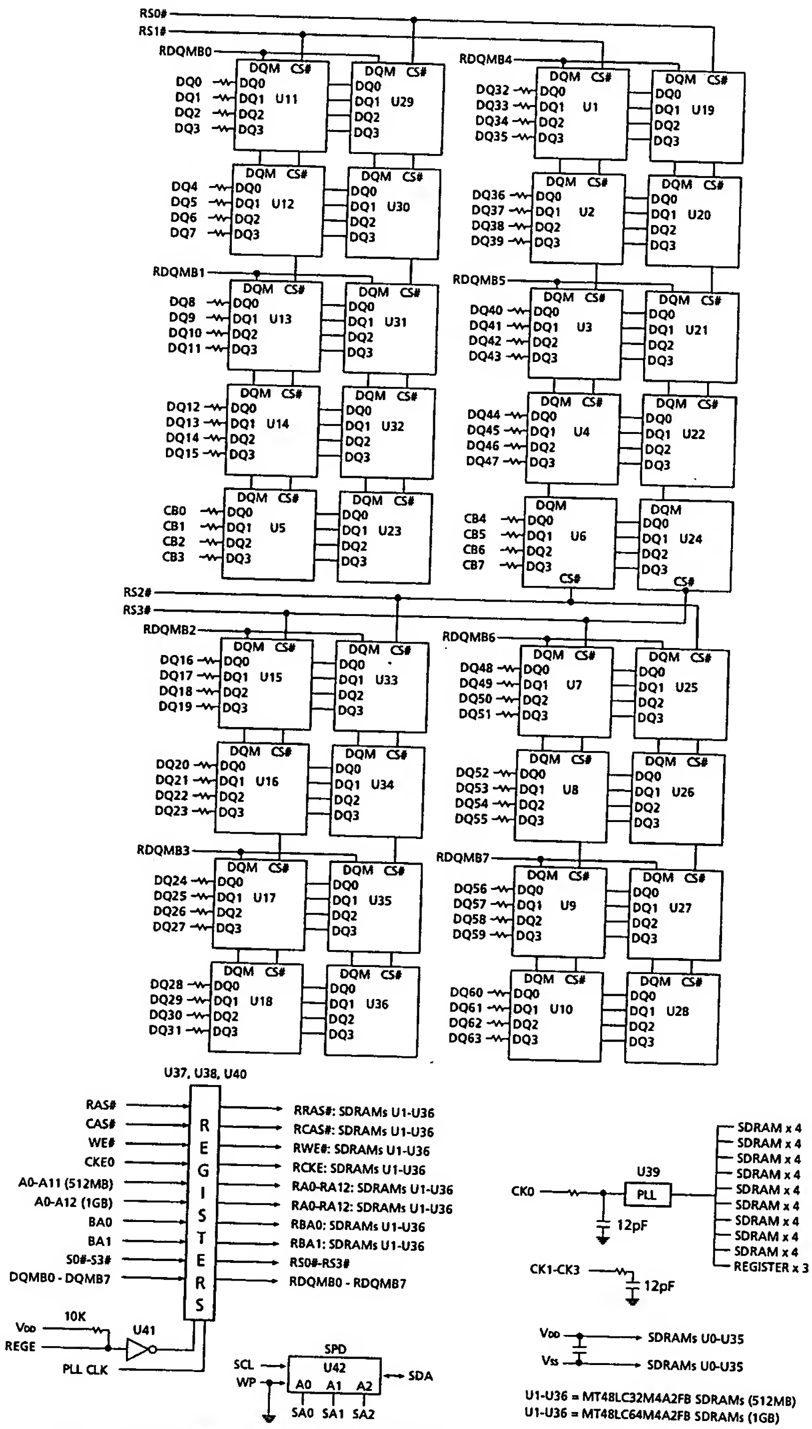
These modules can be operated in either registered mode (REGE pin HIGH), where the control/address input signals are latched in the register on one rising clock edge and sent to the SDRAM devices on the following rising clock edge (data access is delayed by one clock), or in buffered mode (REGE pin LOW) where the input signals pass through the register/buffer to the SDRAM devices on the same clock.

A phase-lock loop (PLL) on the modules is used to redrive the clock to the SDRAM devices to minimize system clock loading. (CK0 is connected to the PLL, and CK1, CK2, and CK3 are terminated.)

SERIAL PRESENCE-DETECT OPERATION

These modules incorporate serial presence-detect (SPD). The SPD function is implemented using a 2,048-bit EEPROM. This nonvolatile storage device contains 256 bytes. The first 128 bytes can be programmed by Micron to identify the module type and various SDRAM organizations and timing parameters. The remaining 128 bytes of storage are available for use by the customer. System READ/WRITE operations between the master (system logic) and the slave EEPROM device (DIMM) occur via a standard IIC bus using the DIMM's SCL (clock) and SDA (data) signals, together with SA(2:0), which provide eight unique DIMM/EEPROM addresses.

FUNCTIONAL BLOCK DIAGRAM
512MB and 1GB Modules



NOTE: 1. All resistor values are 10 ohms unless otherwise specified.

PIN DESCRIPTIONS

PIN NUMBERS	SYMBOL	TYPE	DESCRIPTION
27, 111, 115	RAS#, CAS#, WE#	Input	Command Inputs: RAS#, CAS#, and WE# (along with S0#-S3#) define the command being entered.
42, 79, 125, 163	CK0-CK3	Input	Clock: CK0 is distributed through an on-board PLL to all devices. CK1-CK3 are terminated.
128, 63	CKE0,CKE1	Input	Clock Enable: CKE0 activates (HIGH) and deactivates (LOW) the CK0 signal. Deactivating the clock provides POWER-DOWN and SELF REFRESH operation (all device banks idle) or CLOCK SUSPEND operation (burst access in progress). CKE0 is synchronous except after the device enters power-down and self refresh modes, where CKE0 becomes asynchronous until after exiting the same mode. The input buffers, including CK0, are disabled during power-down and self refresh modes, providing low standby power.
30, 45, 114, 129	S0#-S3#	Input	Chip Select: S0#-S3# enable (registered LOW) and disable (registered HIGH) the command decoder. All commands are masked when S0#-S3# are registered HIGH. S0#-S3# are considered part of the command code.
28, 29, 46, 47, 112, 113, 130, 131	DQMB0-DQMB7	Input	Input/Output Mask: DQMB is an input mask signal for write accesses and an output enable signal for read accesses. Input data is masked when DQMB is sampled HIGH during a WRITE cycle. The output buffers are placed in a High-Z state (two-clock latency) when DQMB is sampled HIGH during a READ cycle.
39, 122	BA0, BA1	Input	Bank Address: BA0 and BA1 define to which device bank the ACTIVE, READ, WRITE, or PRECHARGE command is being applied.
33-38, 117-121, 123, 126	A0-A11 (512MB) A0-A12 (1GB)	Input	Address Inputs: A0-A11/A12 are sampled during the ACTIVE command (row-address A0-A11/A12) and READ/WRITE command (column-address A0-A9, A11, with A10 defining auto precharge) to select one location out of the memory array in the respective device bank. A10 is sampled during a PRECHARGE command to determine if both device banks are to be precharged (A10 HIGH). The address inputs also provide the op-code during a LOAD MODE REGISTER command.
81	WP	Input	Write Protect: Serial presence-detect hardware write protect.
83	SCL	Input	Serial Clock for Presence-Detect: SCL is used to synchronize the presence-detect data transfer to and from the module.
165-167	SA0-SA2	Input	Presence-Detect Address Inputs: These pins are used to configure the presence-detect device.
147	REGE	Input	Register Enable: REGE permits the DIMM to operate in "buffered" mode (LOW) or "registered' mode (HIGH).

NOTE: Pin numbers are listed in module pinout order and do not necessarily correlate with symbols.

PIN DESCRIPTIONS (continued)

PIN NUMBERS	SYMBOL	TYPE	DESCRIPTION
2-5, 7-11, 13-17, 19-20, 55-58, 60, 65-67, 69-72, 74-77, 86-89, 91-95, 97-101, 103-104, 139-142, 144, 149-151, 153-156, 158-161	DQ0-DQ63	Input/ Output	Data I/Os: Data bus.**
21, 22, 52, 53, 105, 106, 136, 137	CB0-CB7	Input/ Output	Check Bits.
82	SDA	Input/ Output	Serial Presence-Detect Data: SDA is a bidirectional pin used to transfer addresses and data into and data out of the presence-detect portion of the module.
6, 18, 26, 40, 41, 49, 59, 73, 84, 90, 102, 110, 124, 133, 143, 157, 168	V_{DD}	Supply	Power Supply: +3.3V ±0.3V.
1, 12, 23, 32, 43, 54, 64, 68, 78, 85, 96, 107, 116, 127, 138, 148, 152, 162	V_{SS}	Supply	Ground.
24, 25, 31, 44, 48 50, 51 61-63, 80, 108, 109, 132, 134, 135, 145, 146, 164	NC	–	Not Connected: Listed pins are not connected on these modules.

NOTE: Pin numbers are listed in module pinout order and do not necessarily correlate with symbols.

SDRAM FUNCTIONAL DESCRIPTION

In general, the 128Mb and 256Mb SDRAM memory devices used for these modules are quad-bank DRAMs, that operate at 3.3V and include a synchronous interface (all signals are registered on the positive edge of the clock signal, CLK). The four banks of a x4, 128Mb device are each configured as 4,096 bit-rows, by 2,048 bit-columns, by 4 input/output bits. The four banks of a x4, 256Mb device are configured as 8,192 bit-rows by 2,048 bit columns, by 4 input/output bits.

Read and write accesses to the SDRAM are burst oriented; accesses start at a selected location and continue for a programmed number of locations in a programmed sequence. Accesses begin with the registration of an ACTIVE command, which is then followed by a READ or WRITE command. The address bits registered coincident with the ACTIVE command are used to select the device bank and row to be accessed BA0 and BA1 select the device bank, A0-A11 (for 128Mb), or A0-A12 (for 256Mb), select the device row. The address bits A0-A9,A11, registered coincident with the READ or WRITE command are used to select the starting device column location for the burst access.

Prior to normal operation, the SDRAM must be initialized. The following sections provide detailed information covering device initialization, register definition, command descriptions and device operation.

Initialization

SDRAMs must be powered up and initialized in a predefined manner. Operational procedures other than those specified may result in undefined operation. Once power is applied to V_{DD} and $V_{DD}Q$ (simultaneously) and the clock is stable (stable clock is defined as a signal cycling within timing constraints specified for the clock pin), the SDRAM requires a 100µs delay prior to issuing any command other than a COMMAND INHIBIT or NOP. Starting at some point during this 100µs period and continuing at least through the end of this period, COMMAND INHIBIT or NOP commands should be applied.

Once the 100µs delay has been satisfied with at least one COMMAND INHIBIT or NOP command having been applied, a PRECHARGE command should be applied. All device banks must then be precharged, thereby placing the device in the all device banks idle state.

Once in the idle state, two auto refresh cycles must be performed. After the auto refresh cycles are complete, the SDRAM is ready for mode register programming. Because the mode register will power up in an unknown state, it should be loaded prior to applying any operational command.

Mode Register Definition

MODE REGISTER

The mode register is used to define the specific mode of operation of the SDRAM. This definition includes the selection of a burst length, a burst type, a CAS latency, an operating mode and a write burst mode, as shown in Mode Register Definition Diagram. The mode register is programmed via the LOAD MODE REGISTER command and will retain the stored information until it is programmed again or the device loses power.

Mode register bits M0-M2 specify the burst length, M3 specifies the type of burst (sequential or interleaved), M4-M6 specify the CAS latency, M7 and M8 specify the operating mode, M9 specifies the write burst mode, and M10 and M11 are reserved for future use. Address A12 (M12) is undefined but should be driven LOW during loading of the mode register.

The mode register must be loaded when all device banks are idle, and the controller must wait the specified time before initiating the subsequent operation. Violating either of these requirements will result in unspecified operation.

Burst Length

Read and write accesses to the SDRAM are burst oriented, with the burst length being programmable, as shown in Mode Register Definition Diagram. The burst length determines the maximum number of column locations that can be accessed for a given READ or WRITE command. Burst lengths of 1, 2, 4, or 8 locations are available for both the sequential and the interleaved burst types, and a full-page burst is available for the sequential type. The full-page burst is used in conjunction with the BURST TERMINATE command to generate arbitrary burst lengths.

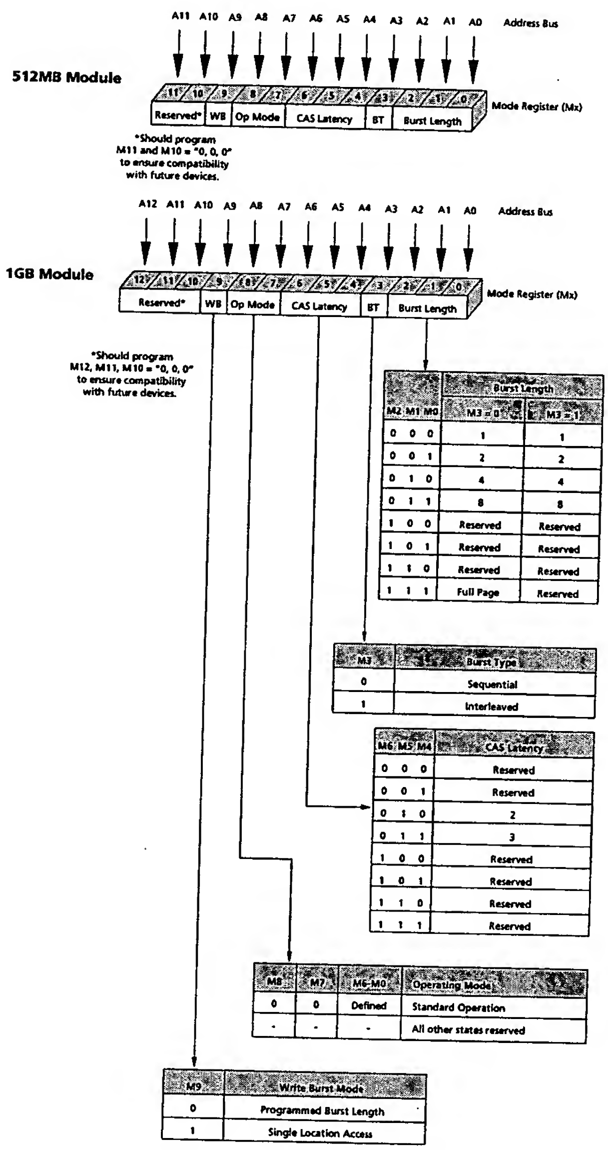
Reserved states should not be used, as unknown operation or incompatibility with future versions may result.

When a READ or WRITE command is issued, a block of columns equal to the burst length is effectively selected. All accesses for that burst take place within this block, meaning that the burst will wrap within the block if a boundary is reached, as shown in the Burst Definition Table The block is uniquely selected by A1-A9, A11 when the burst length is set to two; A2-A9, A11 when the burst length is set to four; and by A3-A9, A11 when the burst length is set to eight. The remaining (least significant) address bit(s) is (are) used to select the starting location within the block. Full-page bursts wrap within the page if the boundary is reached, as shown in the Burst Definition Table.

Burst Typ

Accesses within a given burst may be programmed to be either sequential or interleaved; this is referred to as the burst type and is selected via bit M3.

The ordering of accesses within a burst is determined by the burst length, the burst type and the starting column address, as shown in the Burst Definition Table.



Mod Regist r D finition Diagram

Burst Definition Table

Burst Length	Starting Column Address	Order of Accesses Within a Burst: Type = Sequential	Type = Interleaved
2	A0		
	0	0-1	0-1
	1	1-0	1-0
4	A1 A0		
	0 0	0-1-2-3	0-1-2-3
	0 1	1-2-3-0	1-0-3-2
	1 0	2-3-0-1	2-3-0-1
	1 1	3-0-1-2	3-2-1-0
8	A2 A1 A0		
	0 0 0	0-1-2-3-4-5-6-7	0-1-2-3-4-5-6-7
	0 0 1	1-2-3-4-5-6-7-0	1-0-3-2-5-4-7-6
	0 1 0	2-3-4-5-6-7-0-1	2-3-0-1-6-7-4-5
	0 1 1	3-4-5-6-7-0-1-2	3-2-1-0-7-6-5-4
	1 0 0	4-5-6-7-0-1-2-3	4-5-6-7-0-1-2-3
	1 0 1	5-6-7-0-1-2-3-4	5-4-7-6-1-0-3-2
	1 1 0	6-7-0-1-2-3-4-5	6-7-4-5-2-3-0-1
	1 1 1	7-0-1-2-3-4-5-6	7-6-5-4-3-2-1-0
Full Page (y)	n = A0-A9, A11 (location 0-y)	Cn, Cn+1, Cn+2 Cn+3, Cn+4... ...Cn-1, Cn...	Not supported

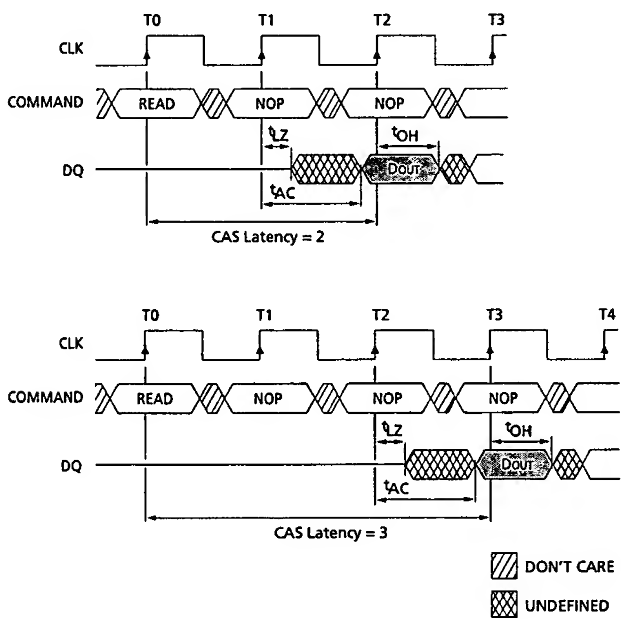
NOTE:
1. For full-page accesses: y = 2,048
2. For a burst length of two, A1-A9, A11 select the block of two burst; A0 selects the starting column within the block.
3. For a burst length of four, A2-A9, A11 select the block of four burst; A0-A1 select the starting column within the block.
4. For a burst length of eight, A3-A9, A11 select the block of eight burst; A0-A2 select the starting column within the block.
5. For a full-page burst, the full row is selected and A0-A9, A11 select the starting column.
6. Whenever a boundary of the block is reached within a given sequence above, the following access wraps within the block.
7. For a burst length of one, A0-A9, A11 select the unique column to be accessed, and Mode Register bit M3 is ignored.

CAS Latency

The CAS latency is the delay, in clock cycles, between the registration of a READ command and the availability of the first piece of output data. The latency can be set to two or three clocks.

If a READ command is registered at clock edge *n*, and the latency is *m* clocks, the data will be available by clock edge $n + m$. The DQs will start driving as a result of the clock edge one cycle earlier ($n + m - 1$), and provided that the relevant access times are met, the data will be valid by clock edge $n + m$. For example, assuming that the clock cycle time is such that all relevant access times are met, if a READ command is registered at T0 and the latency is programmed to two clocks, the DQs will start driving after T1 and the data will be valid by T2, as shown in the CAS Latency Diagram. The CAS Latency Table indicate the operating frequencies at which each CAS latency setting can be used.

Reserved states should not be used as unknown operation or incompatibility with future versions may result.



CAS Latency Diagram

Operating Mode

The normal operating mode is selected by setting M7 and M8 to zero; the other combinations of values for M7 and M8 are reserved for future use and/or test modes. The programmed burst length applies to both READ and WRITE bursts.

Test modes and reserved states should not be used because unknown operation or incompatibility with future versions may result.

Write Burst Mode

When M9 = 0, the burst length programmed via M0-M2 applies to both READ and WRITE bursts; when M9 = 1, the programmed burst length applies to READ bursts, but write accesses are single-location (nonburst) accesses.

CAS Latency Table

SPEED	ALLOWABLE OPERATING FREQUENCY (MHz)	
	CAS LATENCY = 2*	CAS LATENCY = 3*
-13E	≤ 133	≤ 143
-133	≤ 100	≤ 133
-10E	≤ 100	N/A

*Input register will add one extra clock in registered mode.

Commands

The Truth Table provides a quick reference of available commands. This is followed by a written description of each command. For a more detailed description of commands and operations refer to the 128Mb or 256Mb SDRAM datasheets.

TRUTH TABLE – SDRAM Commands and DQMB Operation

(Note: 1, notes appear below table)

NAME (FUNCTION)	CS#	RAS#	CAS#	WE#	DQMB	ADDR	DQs	NOTES
COMMAND INHIBIT (NOP)	H	X	X	X	X	X	X	
NO OPERATION (NOP)	L	H	H	H	X	X	X	
ACTIVE (Select bank and activate row)	L	L	H	H	X	Bank/Row	X	3
READ (Select bank and column, and start READ burst)	L	H	L	H	L/H[8]	Bank/Col	X	4
WRITE (Select bank and column, and start WRITE burst)	L	H	L	L	L/H[8]	Bank/Col	Valid	4
BURST TERMINATE	L	H	H	L	X	X	Active	
PRECHARGE (Deactivate row in bank or banks)	L	L	H	L	X	Code	X	5
AUTO REFRESH or SELF REFRESH (Enter self refresh mode)	L	L	L	H	X	X	X	6, 7
LOAD MODE REGISTER	L	L	L	L	X	Op-Code	X	2
Write Enable/Output Enable	–	–	–	–	L	–	Active	8
Write Inhibit/Output High-Z	–	–	–	–	H	–	High-Z	8

NOTE:
1. CKE is HIGH for all commands shown except SELF REFRESH.
2. A0-A11 (512MB), A0-A12 (1GB) define the op-code written to the Mode Register, and should be driven low.
3. A0-A11 (512MB), A0-A12 (1GB) provide device row address. BA0, BA1 determine which device bank is made active.
4. A0-A9, A11 provide device column address; A10 HIGH enables the auto precharge feature (nonpersistent), while A10 LOW disables the auto precharge feature; BA0, BA1 determine which device bank is being read from or written to.
5. A10 LOW: BA0, BA1 determine which device bank is being precharged. A10 HIGH: both device banks are precharged and BA0, BA1 are "Don't Care."
6. This command is AUTO REFRESH if CKE is HIGH, SELF REFRESH if CKE is LOW.
7. Internal refresh counter controls row addressing; all inputs and I/Os are "Don't Care" except for CKE.
8. Activates or deactivates the DQs during WRITEs (zero-clock delay) and READs (two-clock delay).

ABSOLUTE MAXIMUM RATINGS*

Voltage on V_{DD} Supply
Relative to Vss .... -1V to +4.6V
Voltage on Inputs, NC or I/O Pins
Relative to Vss .... -1V to +4.6V
Operating Temperature, T_A (ambient) ... 0°C to +70°C
Storage Temperature (plastic) .... -55°C to +150°C
Power Dissipation 36W

*Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only, and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

DC ELECTRICAL CHARACTERISTICS AND OPERATING CONDITIONS

(Notes: 1, 5, 6; notes appear following parameter tables); (V_{DD}, $V_{DD}Q$ = +3.3V ±0.3V)

PARAMETER/CONDITION	SYMBOL	MIN	MAX	UNITS	NOTES
SUPPLY VOLTAGE	V_{DD}, $V_{DD}Q$	3	3.6	V	
INPUT HIGH VOLTAGE: Logic 1; All inputs	V_{IH}	2	V_{DD} + 0.3	V	22
INPUT LOW VOLTAGE: Logic 0; All inputs	V_{IL}	-0.3	0.8	V	22
INPUT LEAKAGE CURRENT: Any input 0V ≤ V_{IN} ≤ V_{DD} (All other pins not under test = 0V) For inputs: A0-A11, A12, BA0, BA1, RAS#, CAS#, and WE#	I_I	-10	10	µA	33
INPUT LEAKAGE CURRENT: Any input 0V ≤ V_{IN} ≤ V_{DD} (All other pins not under test = 0V) For inputs: S0#-S3#, DQMB1-DQMB7	I_I	-5	5	µA	33
INPUT LEAKAGE CURRENT: Any input 0V ≤ V_{IN} ≤ V_{DD} (All other pins not under test = 0V) For inputs: CKE0	I_I	-20	20	µA	33
OUTPUT LEAKAGE CURRENT: DQs are disabled; 0V ≤ V_{OUT} ≤ $V_{DD}Q$	I_{OZ}	-10	10	µA	33
OUTPUT LEVELS: Output High Voltage (I_{OUT} = -4mA)	V_{OH}	2.4	–	V	
Output Low Voltage (I_{OUT} = 4mA)	V_{OL}	–	0.4	V	

I_{DD} SPECIFICATIONS AND CONDITIONS* (512MB MODULE)

(Notes: 1, 6, 11, 13; notes appear following parameter tables)
(V_{DD}, $V_{DD}Q$ = +3.3V ±0.3V)

PARAMETER/CONDITION		SYMBOL	MAX -13E	MAX -133	MAX -10E	UNITS	NOTES
OPERATING CURRENT: Active Mode; Burst = 2; READ or WRITE; $^tRC = {}^tRC$ (MIN)		I_{DD1}[a]	2,916	2,736	2,556	mA	3, 18, 19, 30
STANDBY CURRENT: Power-Down Mode; All device banks idle; CKE = LOW		I_{DD2}[b]	72	72	72	mA	30
STANDBY CURRENT: Active Mode; CKE = HIGH; CS# = HIGH; All device banks active after ^tRCD met; No accesses in progress		I_{DD3}[a]	936	936	756	mA	3, 12, 19, 30
OPERATING CURRENT: Burst Mode; Continuous burst; READ or WRITE; All device banks active		I_{DD4}[a]	3,006	2,736	2,556	mA	3, 18, 19, 30
AUTO REFRESH CURRENT CS# = HIGH; CKE = HIGH	$^tRFC = {}^tRFC$ (MIN)	I_{DD5}[b]	11,880	11,160	9,720	mA	3, 12, 18, 19, 30, 31
	^tRFC = 15.6 µs	I_{DD6}[b]	108	108	108	mA	
SELF REFRESH CURRENT: CKE ≤ 0.2V		I_{DD7}[b]	72	72	72	mA	4

I_{DD} SPECIFICATIONS AND CONDITIONS* (1GB MODULE)

(Notes: 1, 6, 11, 13; notes appear following parameter tables)
(V_{DD}, $V_{DD}Q$ = +3.3V ±0.3V)

PARAMETER/CONDITION		SYMBOL	MAX -13E	MAX -133	MAX -10E	UNITS	NOTES
OPERATING CURRENT: Active Mode; Burst = 2; READ or WRITE; $^tRC = {}^tRC$ (MIN)		I_{DD1}[a]	2,466	2,286	2,286	mA	3, 18, 19, 30
STANDBY CURRENT: Power-Down Mode; All device banks idle; CKE = LOW		I_{DD2}[b]	72	72	72	mA	30
STANDBY CURRENT: Active Mode; CKE = HIGH; CS# = HIGH; All device banks active after ^tRCD met; No accesses in progress		I_{DD3}[a]	756	756	1,026	mA	3, 12, 19, 30
OPERATING CURRENT: Burst Mode; Continuous burst; READ or WRITE; All device banks active		I_{DD4}[a]	2,466	2,466	2,736	mA	3, 18, 19, 30
AUTO REFRESH CURRENT CS# = HIGH; CKE = HIGH	$^tRFC = {}^tRFC$ (MIN)	I_{DD5}[b]	10,260	9,720	10,800	mA	3, 12, 18, 19, 30, 31
	^tRFC = 7.81 µs	I_{DD6}[b]	126	126	144	mA	
SELF REFRESH CURRENT: CKE ≤ 0.2V		I_{DD7}[b]	90	90	108	mA	4

*DRAM components only.
a - Value calculated as one module bank in this operating condition, and all other module banks in power-down mode.
b - Value calculated reflects all module banks in this operating condition.

CAPACITANCE (512MB, 1GB)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS
Input Capacitance: A0-A12, BA0, BA1, RAS#, CAS#, WE#	C_{I1}	–	8	–	pF
Input Capacitance: CKE0, CKE1	C_{I2}	–	16	–	pF
Input Capacitance: CK1-CK3	C_{I3}	–	12	–	pF
Input Capacitance: S0#-S3#, DQMB0-DQMB7, CK0	C_{I4}	–	4	–	pF
Input Capacitance: REGE	C_{I5}	-	1.5	12	pF
Input Capacitance: SCL, SA0-SA2	C_{I6}	–	–	10	pF
Input/Output Capacitance: DQ0-DQ63, CB0-CB7, SDA	C_{IO}	6	–	12	pF

NOTE: This parameter is sampled. V_{DD}, $V_{DD}Q$ = +3.3V; f = 1 MHz, T_A = 25°C; pin under test biased at 1.4V.

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS*

(Notes: 5, 6, 8, 9, 11; notes appear following parameter tables)

AC CHARACTERISTICS			-13E		-133		-10E			
PARAMETER		SYMBOL	MIN	MAX	MIN	MAX	MIN	MAX	UNITS	NOTES
Access time from CLK (pos. edge)	CL = 3	$^tAC(3)$		5.4		5.4		6	ns	27
	CL = 2	$^tAC(2)$		5.4		6		6	ns	
Address hold time		^tAH	0.8		0.8		1		ns	
Address setup time		^tAS	1.5		1.5		2		ns	
CLK high-level width		^tCH	2.5		2.5		3		ns	
CLK low-level width		^tCL	2.5		2.5		3		ns	
Clock cycle time	CL = 3	$^tCK(3)$	7		7.5		8		ns	23
	CL = 2	$^tCK(2)$	7.5		10		10		ns	23
CKE hold time		^tCKH	0.8		0.8		1		ns	
CKE setup time		^tCKS	1.5		1.5		2		ns	
CS#, RAS#, CAS#, WE#, DQM hold time		^tCMH	0.8		0.8		1		ns	
CS#, RAS#, CAS#, WE#, DQM setup time		^tCMS	1.5		1.5		2		ns	
Data-in hold time		^tDH	0.8		0.8		1		ns	
Data-in setup time		^tDS	1.5		1.5		2		ns	
Data-out high-impedance time	CL = 3	$^tHZ(3)$		5.4		5.4		6	ns	10
	CL = 2	$^tHZ(2)$		5.4		6		6	ns	10
Data-out low-impedance time		^tLZ	1		1		1		ns	
Data-out hold time (load)		^tOH	3		3		3		ns	
Data-out hold time (no load)		^tOH_N	1.8		1.8		1.8		ns	28
ACTIVE to PRECHARGE command		^tRAS	37	120,000	44	120,000	50	120,000	ns	29
ACTIVE to ACTIVE command period		^tRC	60		66		70		ns	
ACTIVE to READ or WRITE delay		^tRCD	15		20		20		ns	
Refresh period		^tREF		64		64		64	ms	
AUTO REFRESH period		^tRFC	66		66		70		ns	
PRECHARGE command period		^tRP	15		20		20		ns	
ACTIVE bank *a* to ACTIVE bank *b* command		^tRRD	14		15		20		ns	
Transition time		^tT	0.3	1.2	0.3	1.2	0.3	1.2	ns	7
WRITE recovery time		^tWR	1 CLK + 7ns		1 CLK + 7.5ns		1 CLK + 7ns		ns	24
			14		15		15		ns	25
Exit SELF REFRESH to ACTIVE command		^tXSR	67		75		80		ns	20

*Module AC timing parameters comply with PC133 Design Specs, based on component parameters.

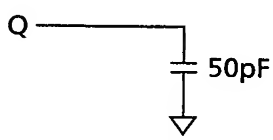
AC FUNCTIONAL CHARACTERISTICS

(Notes: 5, 6, 7, 8, 9, 11; notes appear following parameter tables)

PARAMETER		SYMBOL	-13E	-133	-10E	UNITS	NOTES
READ/WRITE command to READ/WRITE command		^tCCD	1	1	1	^tCK	17
CKE to clock disable or power-down entry mode		^tCKED	1	1	1	^tCK	14, 32
CKE to clock enable or power-down exit setup mode		^tPED	1	1	1	^tCK	14, 32
DQM to input data delay		^tDQD	0	0	0	^tCK	17, 32
DQM to data mask during WRITEs		^tDQM	0	0	0	^tCK	17, 32
DQM to data high-impedance during READs		^tDQZ	2	2	2	^tCK	17, 32
WRITE command to input data delay		^tDWD	0	0	0	^tCK	17, 32
Data-in to ACTIVE command		^tDAL	4	5	4	^tCK	15, 21, 32
Data-in to PRECHARGE command		^tDPL	2	2	2	^tCK	16, 21, 32
Last data-in to burst STOP command		^tBDL	1	1	1	^tCK	17, 32
Last data-in to new READ/WRITE command		^tCDL	1	1	1	^tCK	17, 32
Last data-in to PRECHARGE command		^tRDL	2	2	2	^tCK	16, 21, 32
LOAD MODE REGISTER command to ACTIVE or REFRESH command		^tMRD	2	2	2	^tCK	26
Data-out to high-impedance from PRECHARGE command	CL = 3	$^tROH(3)$	3	3	3	^tCK	17, 32
	CL = 2	$^tROH(2)$	2	2	2	^tCK	17, 32

NOTES

1. All voltages referenced to V_{SS}.
2. This parameter is sampled. V_{DD}, $V_{DD}Q$ = +3.3V; f = 1 MHz, T_A = 25°C; pin under test biased at 1.4V.
3. I_{DD} is dependent on output loading and cycle rates. Specified values are obtained with minimum cycle time and the outputs open.
4. Enables on-chip refresh and address counters.
5. The minimum specifications are used only to indicate cycle time at which proper operation over the full temperature range is ensured; (0°C ≤ T_A ≤ +70°C).
6. An initial pause of 100µs is required after power-up, followed by two AUTO REFRESH commands, before proper device operation is ensured. (V_{DD} and $V_{DD}Q$ must be powered up simultaneously. V_{SS} and $V_{SS}Q$ must be at same potential.) The two AUTO REFRESH command wake-ups should be repeated any time the ^{t}REF refresh requirement is exceeded.
7. AC characteristics assume ^{t}T = 1ns.
8. In addition to meeting the transition rate specification, the clock and CKE must transit between V_{IH} and V_{IL} (or between V_{IL} and V_{IH}) in a monotonic manner.
9. Outputs measured at 1.5V with equivalent load:



10. ^{t}HZ defines the time at which the output achieves the open circuit condition; it is not a reference to V_{OH} or V_{OL}. The last valid data element will meet ^{t}OH before going High-Z.
11. AC timing and I_{DD} tests have V_{IL} = 0V and V_{IH} = 3V, with timing referenced to 1.5V crossover point. If the input transition time is longer than 1 ns, then the timing is referenced at V_{IL} (MAX) and V_{IH} (MIN) and no longer at the 1.5V crossover point. Refer to Micron Technical Note TN-48-09.
12. Other input signals are allowed to transition no more than once every two clocks and are otherwise at valid V_{IH} or V_{IL} levels.
13. I_{DD} specifications are tested after the device is properly initialized.
14. Timing actually specified by ^{t}CKS; clock(s) specified as a reference only at minimum cycle rate.
15. Timing actually specified by ^{t}WR plus ^{t}RP; clock(s) specified as a reference only at minimum cycle rate.
16. Timing actually specified by ^{t}WR.
17. Required clocks are specified by JEDEC functionality and are not dependent on any timing parameter.
18. The I_{DD} current will increase or decrease proportionally according to the amount of frequency alteration for the test condition.
19. Address transitions average one transition every two clocks.
20. CLK must be toggled a minimum of two times during this period.
21. Based on ^{t}CK = 10ns for -10E, and ^{t}CK = 7.5ns for -133 and -13E.
22. V_{IH} overshoot: V_{IH} (MAX) = $V_{DD}Q$ + 2V for a pulse width ≤ 3ns, and the pulse width cannot be greater than one third of the cycle rate. V_{IL} undershoot: V_{IL} (MIN) = -2V for a pulse width ≤ 3ns.
23. The clock frequency must remain constant (stable clock is defined as a signal cycling within timing constraints specified for the clock pin) during access or precharge states (READ, WRITE, including ^{t}WR, and PRECHARGE commands). CKE may be used to reduce the data rate.
24. Auto precharge mode only. The precharge timing budget (^{t}RP) begins 7ns for -13E; 7.5ns for -133 and 7ns for -10E after the first clock delay, after the last WRITE is executed. May not exceed limit set for precharge mode.
25. Precharge mode only.
26. JEDEC and PC100 specify three clocks.
27. ^{t}AC for -133/-13E at CL = 3 with no load is 4.6ns and is guaranteed by design.
28. Parameter guaranteed by design.
29. The value for ^{t}RAS used in -13E speed grade modules is calculated from ^{t}RC - ^{t}RP.
30. For -10E, CL= 2 and ^{t}CK = 10ns; for -133, CL = 3 and ^{t}CK = 7.5ns; for -13E, CL = 2 and ^{t}CK = 7.5ns.
31. CKE is HIGH during refresh command period ^{t}RFC (MIN) else CKE is LOW. The $I_{DD}6$ limit is actually a nominal value and does not result in a fail value.
32. This AC timing function will show an extra clock cycle when in registered mode.
33. Leakage number reflects the worst case leakage possible through the module pin, not what each memory device contributes.

SPD CLOCK AND DATA CONVENTIONS

Data states on the SDA line can change only during SCL LOW. SDA state changes during SCL HIGH are reserved for indicating start and stop conditions (Figures 1 and 2).

SPD START CONDITION

All commands are preceded by the start condition, which is a HIGH-to-LOW transition of SDA when SCL is HIGH. The SPD device continuously monitors the SDA and SCL lines for the start condition and will not respond to any command until this condition has been met.

SPD STOP CONDITION

All communications are terminated by a stop condition, which is a LOW-to-HIGH transition of SDA when SCL is HIGH. The stop condition is also used to place the SPD device into standby power mode.

SPD ACKNOWLEDGE

Acknowledge is a software convention used to indicate successful data transfers. The transmitting device, either master or slave, will release the bus after transmitting eight bits. During the ninth clock cycle, the receiver will pull the SDA line LOW to acknowledge that it received the eight bits of data (Figure 3).

The SPD device will always respond with an acknowledge after recognition of a start condition and its slave address. If both the device and a WRITE operation have been selected, the SPD device will respond with an acknowledge after the receipt of each subsequent eight-bit word. In the read mode the SPD device will transmit eight bits of data, release the SDA line and monitor the line for an acknowledge. If an acknowledge is detected and no stop condition is generated by the master, the slave will continue to transmit data. If an acknowledge is not detected, the slave will terminate further data transmissions and await the stop condition to return to standby power mode.

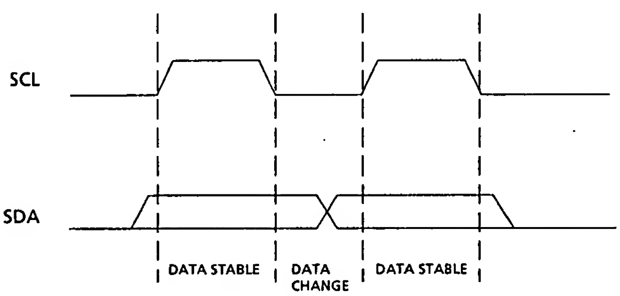


Figure 1
Data Validity

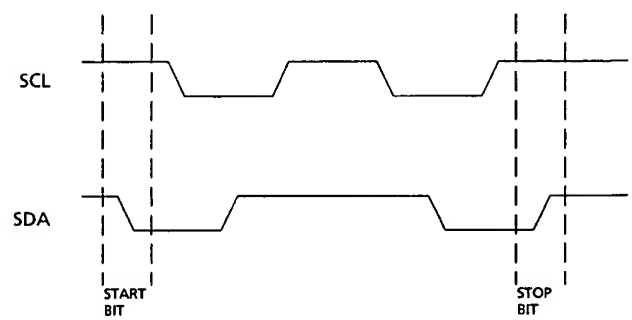


Figure 2
Definition of Start and Stop

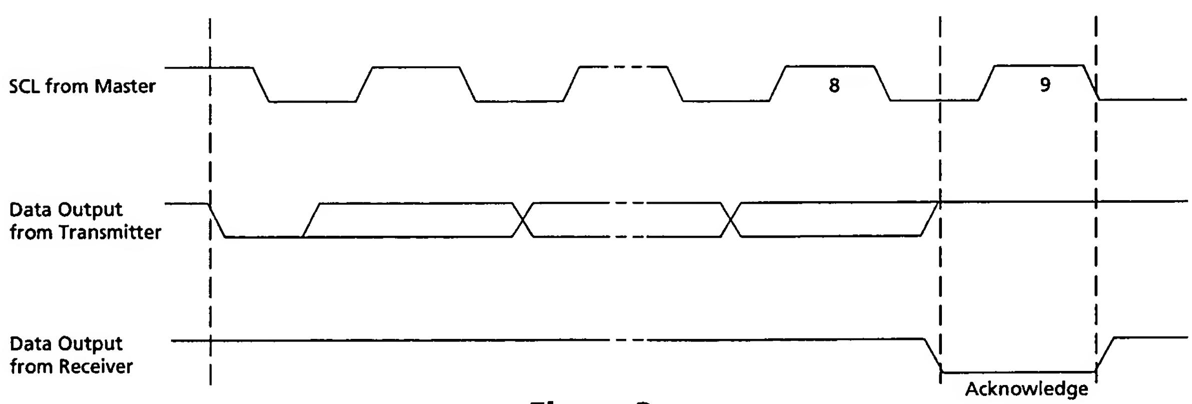


Figure 3
Acknowl dge Resp nse From Receiver

EEPROM DEVICE SELECT CODE

(The most significant bit (b7) is sent first)

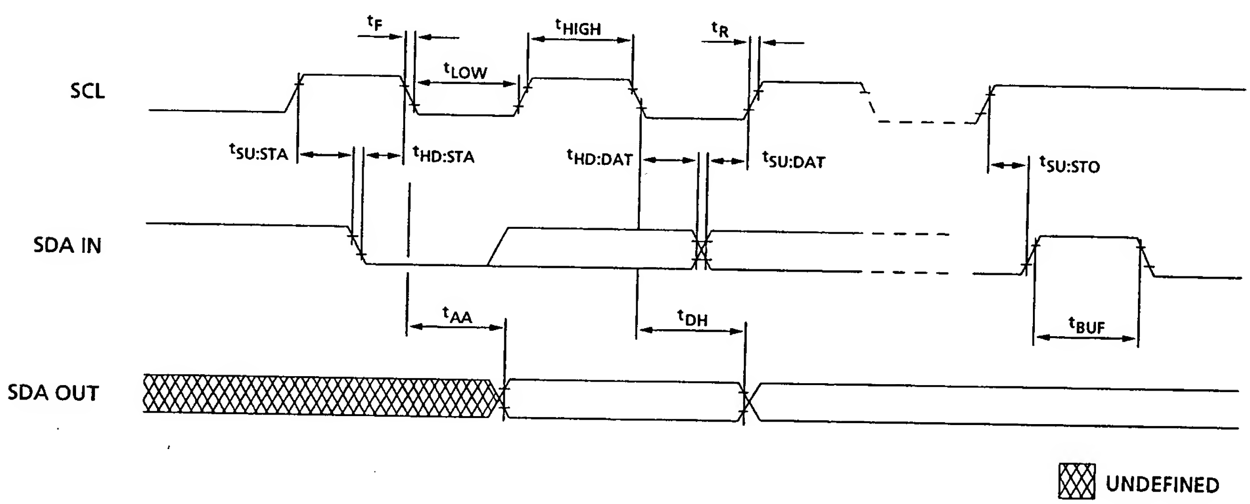
	Device Type Identifier				Chip Enable			RW
	b7	b6	b5	b4	b3	b2	b1	b0
Memory Area Select Code (two arrays)	1	0	1	0	E2	E1	E0	$R\overline{W}$
Protection Register Select Code	0	1	1	0	E2	E1	E0	$R\overline{W}$

EEPROM OPERATING MODES

(X = V_{IH} or V_{IL})

MODE	RW Bit	WC	BYTES	Initial Sequence
Current Address Read	1	X	1	Start, Device Select, $R\overline{W}$ = 1
Random Address Read	0	X	1	Start, Device Select, $R\overline{W}$ = 0, Address
	1	X		reSTART, Device Select, $R\overline{W}$ = 1
Sequential Read	1	X	≥ 1	Similar to Current or Random Address Read
Byte Write	0	V_{IL}	1	START, Device Select, $R\overline{W}$ = 0
Page Write	0	V_{IL}	≤ 16	START, Device Select, $R\overline{W}$ = 0

SPD EEPROM TIMING DIAGRAM



SERIAL PRESENCE-DETECT EEPROM TIMING PARAMETERS

SYMBOL	MIN	MAX	UNITS
t_{AA}	0.3	3.5	µs
t_{BUF}	4.7		µs
t_{DH}	300		ns
t_F		300	ns
$t_{HD:DAT}$	0		µs
$t_{HD:STA}$	4		µs

SYMBOL	MIN	MAX	UNITS
t_{HIGH}	4		µs
t_{LOW}	4.7		µs
t_R		1	µs
$t_{SU:DAT}$	250		ns
$t_{SU:STA}$	4.7		µs
$t_{SU:STO}$	4.7		µs

SERIAL PRESENCE-DETECT EEPROM DC OPERATING CONDITIONS

(Note: 1) (V_{DD} = +3.3V ±0.3V)

PARAMETER/CONDITION	SYMBOL	MIN	MAX	UNITS
SUPPLY VOLTAGE	V_{DD}	3	3.6	V
INPUT HIGH VOLTAGE: Logic 1; All inputs	V_{IH}	V_{DD} x 0.7	V_{DD} + 0.5	V
INPUT LOW VOLTAGE: Logic 0; All inputs	V_{IL}	-1	V_{DD} x 0.3	V
OUTPUT LOW VOLTAGE: I_{OUT} = 3mA	V_{OL}	–	0.4	V
INPUT LEAKAGE CURRENT: V_{IN} = GND to V_{DD}	I_{LI}	–	10	µA
OUTPUT LEAKAGE CURRENT: V_{OUT} = GND to V_{DD}	I_{LO}	–	10	µA
STANDBY CURRENT: SCL = SDA = V_{DD} - 0.3V; All other inputs = GND or 3.3V +10%	I_{SB}	–	30	µA
POWER SUPPLY CURRENT: SCL clock frequency = 100 KHz	I_{DD}	–	2	mA

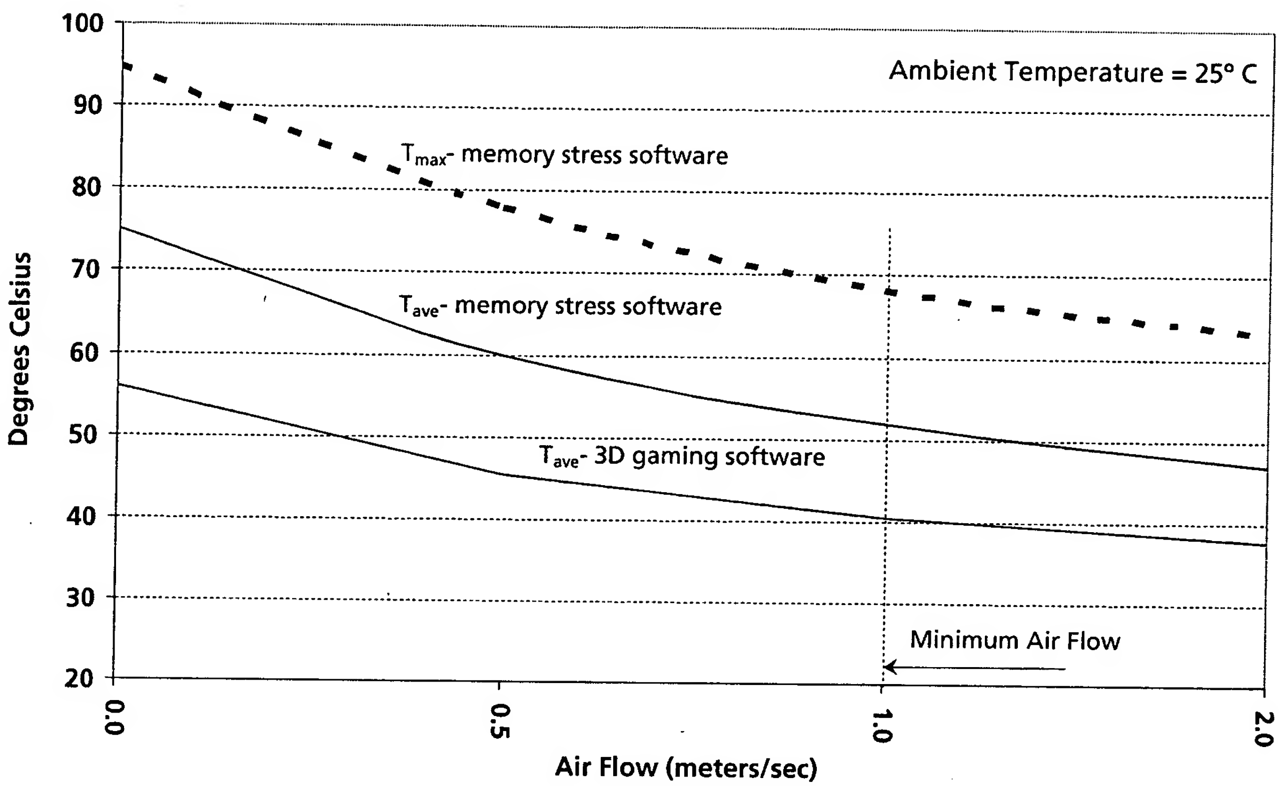
SERIAL PRESENCE-DETECT EEPROM AC OPERATING CONDITIONS

(Note: 1) (V_{DD} = +3.3V ±0.3V)

PARAMETER/CONDITION	SYMBOL	MIN	MAX	UNITS	NOTES
SCL LOW to SDA data-out valid	^tAA	0.3	3.5	µs	
Time the bus must be free before a new transition can start	^tBUF	4.7		µs	
Data-out hold time	^tDH	300		ns	
SDA and SCL fall time	^tF		300	ns	
Data-in hold time	$^tHD:DAT$	0		µs	
Start condition hold time	$^tHD:STA$	4		µs	
Clock HIGH period	^tHIGH	4		µs	
Noise suppression time constant at SCL, SDA inputs	^tI		100	ns	
Clock LOW period	^tLOW	4.7		µs	
SDA and SCL rise time	^tR		1	µs	
SCL clock frequency	^tSCL		100	KHz	
Data-in setup time	$^tSU:DAT$	250		ns	
Start condition setup time	$^tSU:STA$	4.7		µs	
Stop condition setup time	$^tSU:STO$	4.7		µs	
WRITE cycle time	^tWRC		10	ms	2

N TE: 1. All voltages referenced to Vss.
2. The SPD EEPROM WRITE cycle time (^tWRC) is the time from a valid stop condition of a write sequence to the end of the EEPROM internal erase/program cycle. During the WRITE cycle, the EEPROM bus interface circuit is disabled, SDA remains HIGH due to pull-up resistor, and the EEPROM does not respond to its slave address.

COMPONENT CASE TEMPERATURE VS. AIR FLOW



NOTE:
1. Micron Technology, Inc. specifies a minimum air flow of 1 meter/second (~197 LFM) across the MT36LSDF6472G and MT36LSDT12872G modules when installed in a system.
2. The component case temperature measurements shown above are obtained experimentally. The system used for experimental purposes is a dual-processor 600 MHz work station, fully loaded with four MT36LSDF6472G modules. Case temperatures charted represent worst-case component locations on modules installed in the internal slots of the system.
3. Temperature versus air speed data is obtained by performing experiments with the system motherboard removed from its case and mounted in a Eiffel-type low air speed wind tunnel. Peripheral devices installed on the system motherboard for testing are the processor(s) and video card, all other peripheral devices are mounted outside of the wind tunnel test chamber.
4. The memory diagnostic software used for determining worst-case component temperatures is a memory diagnostic software application developed for internal use by Micron Technology, Inc.

SERIAL PRESENCE-DETECT MATRIX

(Note: 1)

BYTE	DESCRIPTION	ENTRY (VERSION)	MT36LSDF6472G	MT36LSDF12872G
0	NUMBER OF BYTES USED BY MICRON	128	80	80
1	TOTAL NUMBER OF SPD MEMORY BYTES	256	08	08
2	MEMORY TYPE	SDRAM	04	04
3	NUMBER OF ROW ADDRESSES	12 or 13	0C	0D
4	NUMBER OF COLUMN ADDRESSES	11	0B	0B
5	NUMBER OF BANKS		2	02 02
6	MODULE DATA WIDTH	72	48	48
7	MODULE DATA WIDTH (continued)	0	00	00
8	MODULE VOLTAGE INTERFACE LEVELS	LVTTL	01	01
9	SDRAM CYCLE TIME, ^{t}CK (CAS LATENCY = 3) (note 2)	7 (-13E) 7.5 (-133) 8 (-10E)	70 75 80	70 75 80
10	SDRAM ACCESS FROM CLOCK, ^{t}AC (CAS LATENCY = 3)	5.4 (-13E/-133) 6 (-10E)	54 60	54 60
11	MODULE CONFIGURATION TYPE	ECC	02	02
12	REFRESH RATE/TYPE	15.6µs/SELF / 7.81µs/SELF	80	82
13	SDRAM WIDTH (PRIMARY SDRAM)	4	04	04
14	ERROR-CHECKING SDRAM DATA WIDTH	4	04	04
15	MIN. CLOCK DELAY FROM BACK-TO-BACK RANDOM COLUMN ADDRESSES, ^{t}CCD	1	01	01
16	BURST LENGTHS SUPPORTED	1, 2, 4, 8, PAGE	8F	8F
17	NUMBER OF BANKS ON SDRAM DEVICE	4	04	04
18	CAS LATENCIES SUPPORTED	2, 3	06	06
19	CS LATENCY	0	01	01
20	WE LATENCY	0	01	01
21	SDRAM MODULE ATTRIBUTES	-13E/-133 -10E	1F 1F	1F 1F
22	SDRAM DEVICE ATTRIBUTES: GENERAL	0E	0E	0E
23	SDRAM CYCLE TIME, ^{t}CK (CAS LATENCY = 2) (note 2)	7.5 (-13E) 10 (-133/-10E)	75 A0	75 A0
24	SDRAM ACCESS FROM CLK, ^{t}AC (CAS LATENCY = 2) (note 2)	5.4 (-13E) 6 (-10E)	54 60	54 60
25	SDRAM CYCLE TIME, ^{t}CK (CAS LATENCY = 1)	-	00	00
26	SDRAM ACCESS FROM CLK, ^{t}AC (CAS LATENCY = 1)	-	00	00
27	MINIMUM ROW PRECHARGE TIME, ^{t}RP	15 (-13E) 20 (-133/-10E)	0F 14	0F 14
28	MINIMUM ROW ACTIVE TO ROW ACTIVE, ^{t}RRD	14 (-13E) 15 (-133) 20 (-10E)	0E 0F 14	0E 0F 14
29	MINIMUM RAS# TO CAS# DELAY, ^{t}RCD	15 (-13E) 20 (-133/-10E)	0F 14	0F 14

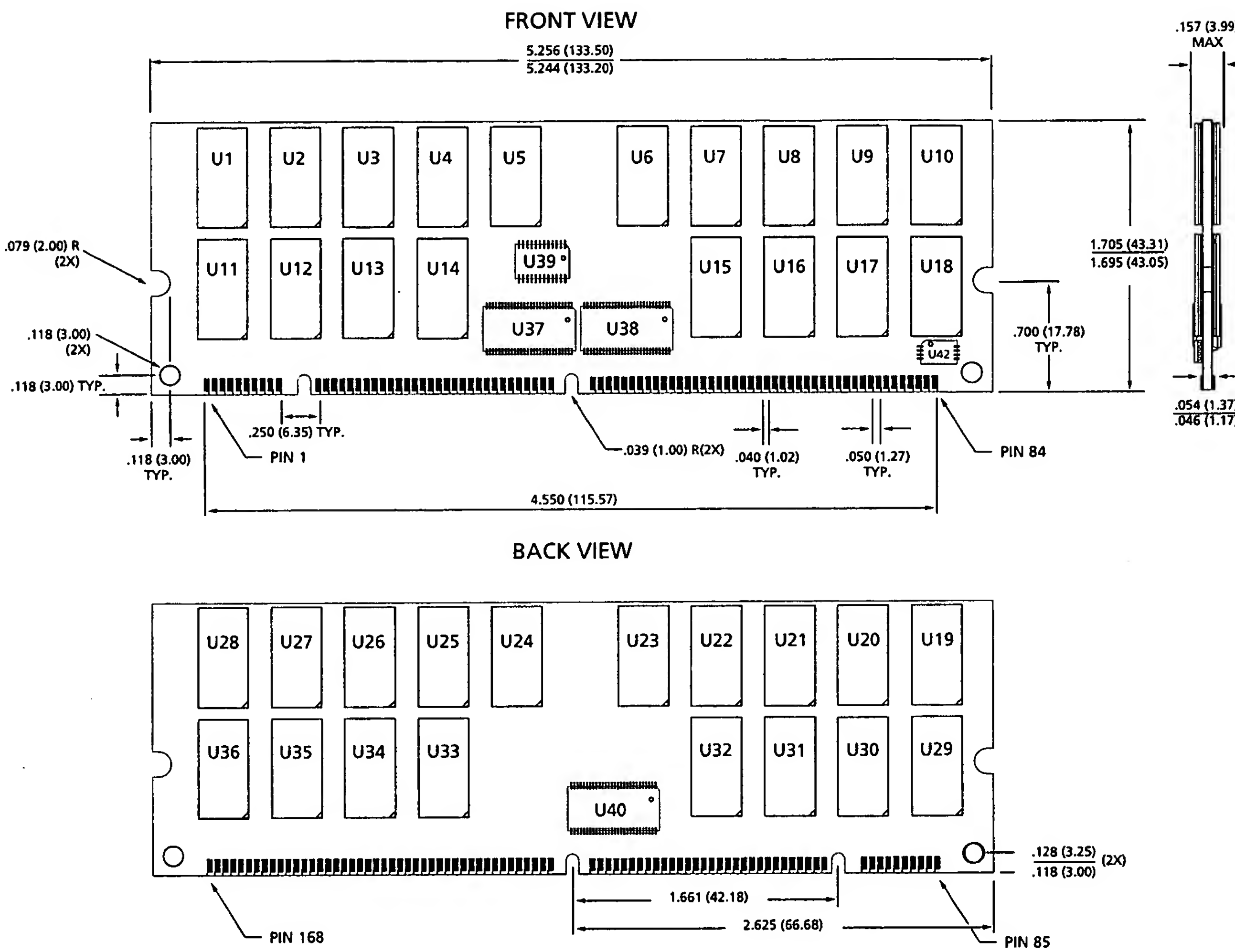
NOTE: 1. "1"/"0": Serial Data, "driven to HIGH"/"driven to LOW."

SERIAL PRESENCE-DETECT MATRIX (continued)

(Notes: 1, 2)

BYTE	DESCRIPTION	ENTRY (VERSION)	MT36LSDF6472G	MT36LSDF12872G
30	MINIMUM RAS# PULSE WIDTH, ^tRAS (note 3)	45 (-13E) 44 (-133) 50 (-10E)	2D 2C 32	2D 2C 32
31	MODULE BANK DENSITY	256MB / 512MB	40	80
32	COMMAND AND ADDRESS SETUP TIME, ^tAS, ^tCMS	1.5 (-13E/-133) 2 (-10E)	15 20	15 20
33	COMMAND AND ADDRESS HOLD TIME, ^tAH, ^tCMH	0.8 (--13E/133) 1 (-10E)	08 10	08 10
34	DATA SIGNAL INPUT SETUP TIME, ^tDS	1.5 (-13E/-133) 2 (-10E)	15 20	15 20
35	DATA SIGNAL INPUT HOLD TIME, ^tDH	0.8 (-13E/-133) 1 (-10E)	08 10	08 10
36-61	RESERVED		00	00
62	SPD REVISION	REV. 1.2	12	12
63	CHECKSUM FOR BYTES 0-62	-13E -133 -10E	B3 F9 41	F6 3C 84
64	MANUFACTURER'S JEDEC ID CODE	MICRON	2C	2C
65-71	MANUFACTURER'S JEDEC ID CODE (CONT.)		FF	FF
72	MANUFACTURING LOCATION		01 02 03 04 05 06 07 08 09	01 02 03 04 05 06 07 08 09
73-90	MODULE PART NUMBER (ASCII)		xx	xx
91	PCB IDENTIFICATION CODE	1 2 3 4 5 6 7 8 9	01 02 03 04 05 06 07 08 09	01 02 03 04 05 06 07 08 09
92	IDENTIFICATION CODE (CONT.)	0	00	00
93	YEAR OF MANUFACTURE IN BCD		xx	xx
94	WEEK OF MANUFACTURE IN BCD		xx	xx
95-98	MODULE SERIAL NUMBER		xx	xx
99-125	MANUFACTURER-SPECIFIC DATA (RSVD)		–	–
126	SYSTEM FREQUENCY	100/133 MHz	64	64
127	SDRAM COMPONENT AND CLOCK DETAIL		8F	8F

NOTE:
1. "1"/"0": Serial Data, "driven to HIGH"/"driven to LOW."
2. x = Variable Data.
3. The value of ^tRAS used for the -13E module is calculated from ^tRC - ^tRP. Actual device spec. value is 37ns.



N TE: All dimensions in inches (millimeters) $\frac{\text{MAX}}{\text{MIN}}$ or typical where noted.

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